# Circuit Modeling of the LM124 Operational Amplifier for Analog Single-Event Transient Analysis

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*Abstract--* **This work presents the development of a transistor-level circuit model of the LM124 operational amplifier specifically engineered and calibrated for analog single-event transient (ASET) computer simulations. The techniques presented rely heavily on datasheet specifications for electrical parameterization and experimental laser probing for dc and transient calibration. The resulting circuit model proves to be suitable for broad-beam SET predictions and fault diagnostics for space applications.**

## I. INTRODUCTION

COMPUTER simulation can play an important role in the study of Analog Single Event Transient (ASET) phenomena in integrated linear circuits. While not a replacement for empirical testing, the cost and time efficiency of simulation make it an attractive complement to traditional experimentation like heavy ion beam tests. Simulations are unrestrictive in choice of test conditions or possible circuit applications. Simulations provide the ability to study internal response mechanisms that may not be experimentally accessible. Simulations can help guide testing procedures and aid with the interpretation of test data. Adequately detailed and verified simulation models can extrapolate a limited set of test data to new operating conditions or applications for the part.

Because analog single event transients can induce internal circuit responses outside the design criteria (e.g. an unanticipated node voltage magnitude, a frequency component outside design specifications, or a bias point destabilization), we have found that normal electrical design models do not adequately model ASET effects. Manufacturer-supplied design data, macromodels, or simplified schematics are engineered for functional circuit design (of the application in which the device is to be used). These models, while useful

for their intended purpose, do not provide the specific details (discussed in this paper) needed for ASET analysis.

We are presently developing ASET circuit models and using circuit simulations to support a comprehensive experimental and analytical characterization study of the ASET response of several common integrated linear circuits in preparation for potential space deployment. Voltage comparators have received SET attention in the literature [1-4]. The understanding of ASET in several of these comparators (e.g. the LM111 and the LM119) has benefited from analyses provided by SET circuit simulation [5-9]. A recent emphasis in computer-assisted SET analysis has been the LM124, an operational amplifier widely used in space applications [6-11]. Unlike the LM111 and LM119, this operational amplifier is the first analog microcircuit for which a full transistor-level circuit model has been developed, calibrated, and verified for predictive ASET analysis.

Development of circuit models for ASET analysis is a relatively new endeavor, and not well developed in the literature. We present here our comprehensive procedure for the construction of a detailed analog integrated circuit model that is formulated, calibrated, and tested specifically for ASET analyses.

This paper has two main objectives: 1) describe in detail the techniques that lead to the development of an accurate transistor-level model of the LM124 operational amplifier for ASET computer simulation, and 2) highlight critical elements that were uncovered during the circuit modeling process requiring special attention to achieve a reliable, predictive tool for the support of ASET characterization prior to space deployment.

First, we present the relevant aspects of the circuit modeling necessary to achieve the Typical Performance Characteristics (TPC) response (the normal electrical operation or datasheet curves) specified by the manufacturer. The choices of the selected specification curves used for these electrical calibrations of the circuit model response, trough the implementation of the transistor libraries, are individually justified. Verification of the model against targeted manufacturer-published responses assured us of the ability of the model to faithfully reproduce particular ac (frequency) or transient responses, which are essential to model the ASET signals.

Then, further refinements were exercised by carefully probing and calibrating the model to experimental laser ASET response data at key nodes. We found the laser an essential tool in the diagnosing of parasitic elements within the circuit; these parasitics were found to be crucial to the accuracy of our ASET modeling. Laser test results were verified over various transistors and multiple amplitudes of transients.

We also used ion microbeam experiments as a validation tool. These targeted tests showed that the circuit model, once diagnosed and calibrated with laser SET data, was able to reproduce heavy ion generated SETs with a high level of accuracy. A comparison over several transistors of the circuit indicated an excellent correlation in the SET output waveforms, as well as in the deposited charge at the junctions of test.

Finally, we validated the LM124 ASET model by comparing computer simulations to broad-beam SET data taken over test conditions different from the conditions used in the previous diagnosis and verification steps. Results showed high fidelity predictions of the broadbeam results. But, more importantly, the model allowed the broadbeam data to be interpreted - trends seen in the broadbeam data were accurately identified and attributed to specific sections of the LM124 circuit, a result that would not have been possible with the broadbeam data in absence of the modeling efforts.

## II. ELECTRICAL RESPONSE CALIBRATION OF THE LM124 OPERATIONAL AMPLIFIER

The LM124 is a high gain operational amplifier (DC voltage gain of 100 dB) and is internally frequency compensated for unity gain at 1MHz. Operational amplifiers, as well as other linear circuits, are often specified and described by simplified circuit schematics and broad definitions of electrical responses from manufacturer-supplied datasheets. These simplified circuit descriptions, or high-level macromodels, are quite useful for simulations of the linear part under normal operating conditions and provide fairly accurate electrical response results for application engineering in most cases. However, we have found that datasheet schematics for the 124-series op amps do not accurately model the unusual effects introduced by a single event – a more complete circuit description is *required*. Consequently, we have developed a complete device-by-device circuit netlist for the LM124 and calibrated the transistor device model parameters for proper electrical operation as specified by the datasheets [12]. In particular, we focused our electrical calibration efforts on the large and small signal response of the circuit – this choice driven by the fact that an SET ion strike induces an electrical response with two particular characteristics: nonlinear voltage swings (large-signal response) and high-frequency signal spectra (small-signal response). So, in addition to information obtained from manufacturer datasheets and conventional analog design practices, we refined useful layout and circuit topology information from the LM124 photomicrograph, shown in Fig. 1, and we proceeded to a laboratory electrical characterization and model calibration for the device.
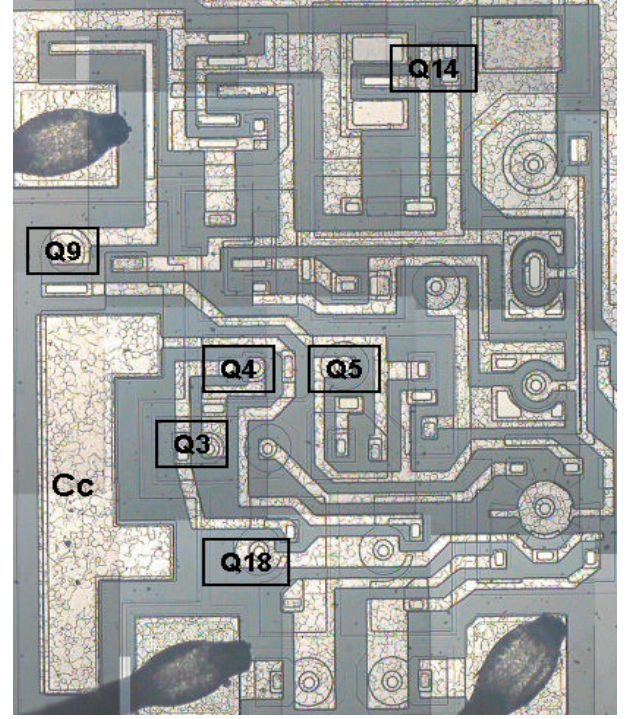


Fig. 1 Photomicrograph of the LM124 operational amplifier used to refine the layout and the topology of the circuit.

### A. Large Signal Pulse Response Calibration

For large signal electrical calibration, the model was placed in the circuit configuration specified by the manufacturer to test the validity of the typical large signal response of an LM124; that is, a voltage follower configuration (unity gain), with a resistive load of 1.8 Kohms and a positive supply voltage of 15 volts. A large signal voltage pulse (2.5 volts in amplitude and 15μs in duration) was applied on the positive input of the amplifier. The calibration of the circuit to the large signal pulse response is very useful to guide the early stages of the modeling process. It is an effective way to verify proper internal biasing and operating points of the modeled layout. More importantly, from the SET analysis perspective, it confirms the ability of the model to adequately respond to large transient voltage swings, such as those occurring during ASETs. Several elements appear to have a dramatic influence on the response of the circuit.

The scaling factors of transistors implemented in the SPICE netlist ([13]) were found to be critical for large signal response fitting. Scaling factors are the ratio of the modeled transistor emitter areas or perimeters to the Chip Test Pattern (CTP) transistors, representative of the process (shown in Fig. 2). The areas of all NPNs and substrate PNPs of the LM124 circuit were measured and ratioed to the NPN or substrate PNP CTPs, and the perimeters of all lateral PNPs were measured and ratioed to the emitter perimeter of the lateral PNP CTP transistor. A correct calculation of these ratios on all the transistors of the circuit is mandatory to realistically reproduce the existing differences in dimensions on the layout. They have an immediate consequence on the current sinking of each transistor, hence on the conduction mode in which each transistor operates. An error in the scaling factor

of transistors leads to incorrect internal biasing, having the consequence of unrealistic circuit operation, or even preventing the simulator from converging.
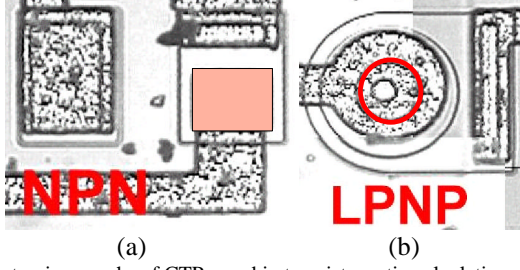


(a)                    (b)

Fig. 2 Photomicrographs of CTPs used in transistor ratio calculations: (a) emitter area for NPN and Substrate PNP, (b) emitter perimeter for Lateral PNP

The LM124, being internally frequency compensated, has a feedback capacitance across the gain stage. Estimation of the value of this compensating capacitor (Cc) is also a major large signal calibration issue. It has a direct influence on the speed of the circuit by strongly affecting both slew rate and stability. Simulations helped us to estimate an optimal value for Cc of 18pF. Fig. 3 shows the comparison between the measured large signal response and the simulated one, calibrated with the adequate scaling factors and Cc=18pF.
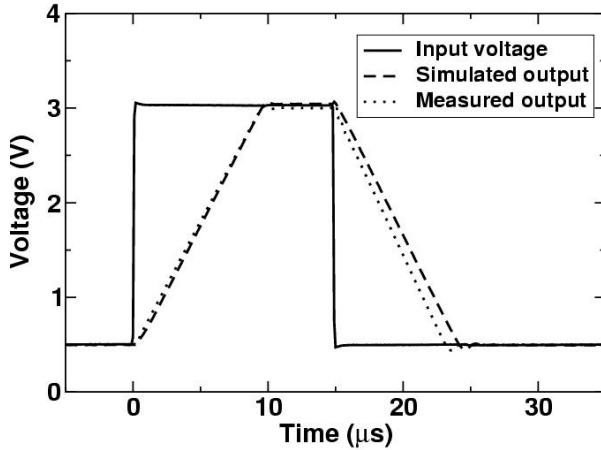


Fig. 3 Comparison between measured and simulated LM124 large signal pulse response.

### B. Small Signal Pulse Response Calibration

For small signal electrical calibration, the model was again simulated in a circuit configuration presented in the manufacturer datasheets as the preferred test configuration for the small signal response. This test consisted in a voltage follower configuration but with a capacitive load of 50pF and a positive supply voltage of 30 volts. This time, a small signal square wave was used as the input voltage on the positive pin (100mv in amplitude and 5μs in duration). The small signal calibration aims at improving the frequency response of the model for a range of frequencies higher than in the previous large signal calibration. The goal for the SET analysis is to gain enough sensitivity to realistically reproduce the high frequency effects induced by the very brief current pulses generated by ion strikes.

Small signal calibrations affected mainly the Modified Gummel-Poon BJT Model parameters of the transistors used in SPICE simulator library. To perform the parameter extraction, the HP 4156 signal analyzer and the HP 4284 LCR meter, used for C-V measurements, were coupled to UTMOST III characterization software [14]. The critical element of this small signal calibration resides in the identification of the parasitics that can affect the transistor model extraction.

At the measurement level, the parasitics are present in the experimental setup - the characterization equipment, the circuit boards and the cables used to interconnect all the apparatuses are inducing capacitive and resistive interferences. These experimentally induced parasitics can be measured and accounted for, by the correcting functions available on the LCR meter (open-short corrections).

At the software level, the choice of transistor electrical characteristics as well transistor parameters appeared to be important. UTMOST parameter extraction routines consist in fitting measured I-V and C-V characteristics to simulated curves from iteratively calculated parameters. We found that the extraction of the basic parameters like $I_S$, $\beta_F$, $N_F$, $V_{AF}$, $I_{KF}$, relative to the forward characteristics - forward Gummel ($I_C$, $I_B$ vs. $V_{BE}$), forward Beta ($\beta_F$ vs. $I_C$) and $I_C$ vs. $V_{CE}$ – is not sufficient. The transistor libraries have to be completed by the reverse ($\beta_R$, $N_R$, $V_{AR}$, $I_{KR}$) and the saturation ($I_{SE}$, $N_E$, $I_{SC}$, $N_C$) condition parameters, using reverse Gummel ($I_E$, -$I_B$ vs. $V_{BC}$), reverse Beta ($\beta_R$ vs. $I_E$) and $I_E$ vs. $V_{EC}$ characteristics.

With careful consideration of experimentally induced parasitic capacitances and the extraction of a complete set of transistor parameters, UTMOST results presented very reasonable small signal response fits. A few mismatches still appeared during the evaluation of some junction capacitances and required manual calibration. Their optimization appeared to be critical for small signal response stability. Fig. 4 shows the result of small signal calibration of the model, after optimizing all junction capacitances.
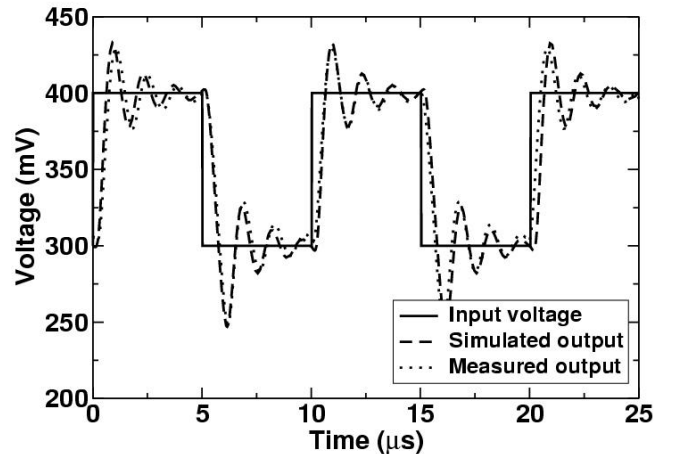


Fig. 4 Comparison between measured and simulated LM124 small signal pulse response.

### III. MODEL CALIBRATION TO LASER SET DATA

The electrical calibration of the LM124 circuit netlist (topology) and transistor model parameters resulted in a circuit that accurately reproduced typical performance specifications stated by the manufacturer and the large and small signal electrical measurements performed in the laboratory. But, to realistically take into account the unique transient effects introduced by SET current pulses, we found that further calibration of the circuit response against actual analog SET data is needed.

Laser tests were performed on the LM124 at the NRL Pulsed Laser SEE Test Facility, which is described in detail elsewhere [16,17]. The pulsed-laser irradiations had a nominal duration of 1 ps at 590 nm (2.1 eV) and pulse repetition rates of 1 to 10 Hz. All experiments were performed at room temperature (295K). The optical pulses were focused onto the device under test with a 100x microscope objective, resulting in a measured Gaussian spot size of 1.2 at the surface of the circuit, which was mounted on a motorized xyz stage with 0.1 resolution. For the experiments reported here, the laser position and focus were optimized to produce the largest amplitude signals.

The experimental test configuration was an inverting amplifier, with a closed loop gain of –20. Fig. 5 shows the circuit configuration used for the test device. During the experiment, several transistors were exposed to laser pulses with a range of pulse energies. Recorded output voltage waveforms showed a large variety of shapes, amplitudes and time widths depending on the laser spot location and pulse energy. It was clear that each of the stages of the amplifier had its own unique and characteristic response to ASETs [15]. The transient response of the model required focussed calibration (aided by the laser) to voltage transients generated in each of the three operational amplifier stages.
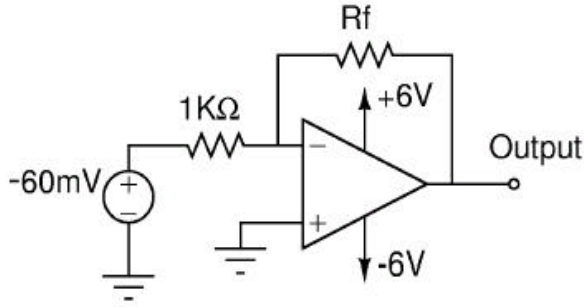


Fig. 5 LM124 inverting circuit configuration used in laser tests. The value of the feedback resistor Rf used is 20 Kohms, providing a closed loop voltage gain of –20 V/V

Calibration to laser SET data helped us to refine parameters showing a strong sensitivity to transient variations of voltages and currents in the circuit – primarily several transistor junction capacitances and parameters for which UTMOST electrical calibration made an average fit – that did not induce a noticeable effect on basic electrical response of the model. Figure 6 shows the importance of laser calibration in refining such parameters: a slight mismatch in the

estimation of one of the capacitances in the transistor model of Q9 - here, the Base-Collector zero-bias depletion capacitance (Cjc)- can result in major variations in output voltage waveforms. However, despite the very significant effect evident in the data of Fig. 6, variations in transistor capacitances shown a negligible effect on previous electrical response calibrations. We see once again how strongly SET analysis can be affected by parasitics. Hence the importance of taking them in account.
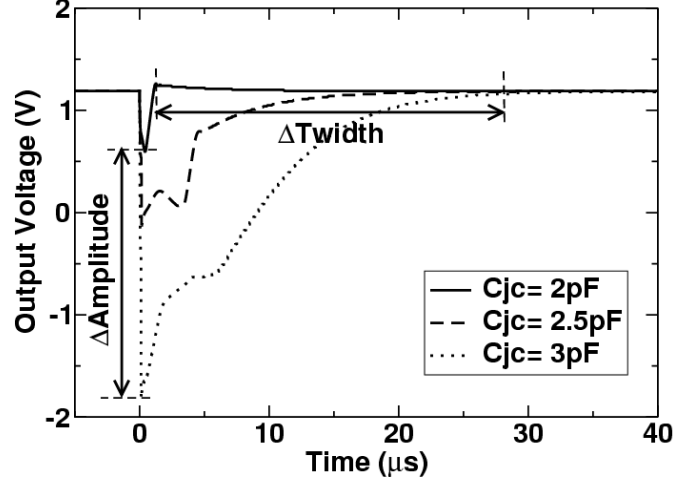


Fig.6 Variations in SETs observed at the output of LM124 model due to a mismatch in the evaluation of the Collector-Base junction capacitance of Q9. The integrated charge of the pulse used for simulation is 20 pC in all three cases, only the value of the capacitance is changed. This case presents a variation in voltage amplitude of 2.4 volts and a variation in pulse width of more than 25 µs.

Figures 7(a), (b) and (c) show the results following careful internal laser probing to identify important parasitics within the device that influence SET response. The figures compare laser SET data with simulations performed on the calibrated model, for two values of collected charge and for transistors Q4, Q9 and Q14 located respectively in the input, amplifier and output stages.

We observe a very good agreement in the general trend of the transient waveforms, amplitudes and pulse widths. According to these positive results after laser SET calibration, we can presume that the use of this transistor-level model for ASET prediction can be extended to other applications based on the LM124 but with different functional configurations.
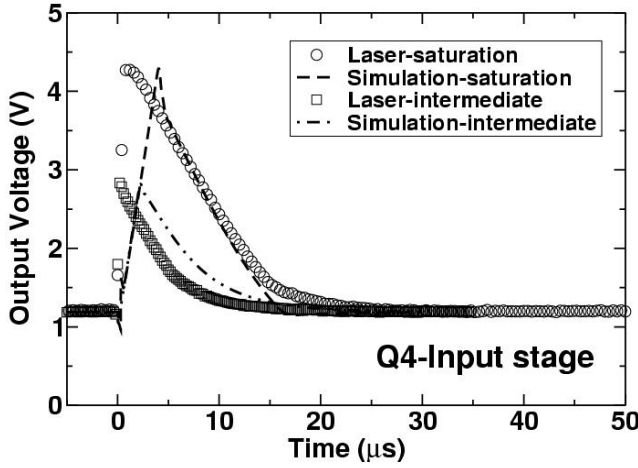
Fig. 7(a) Output voltage transients for a laser strike to transistor Q4 in the input stage of the LM124. The laser was simulated by a current source applied at the Collector-Base junction, with a total integrated charge of 15 pC for the intermediate transient and 100 pC for the saturating transient.
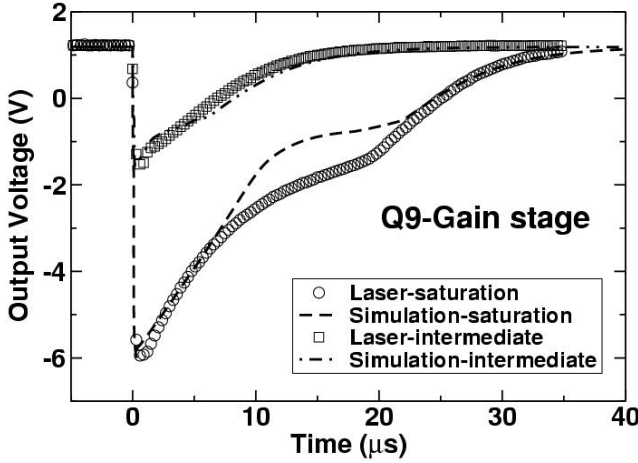


Fig. 7(b) Output voltage transients for a laser strike to transistor Q9 in the amplifier stage of the LM124 The laser was simulated by a current source applied at the Collector-Base junction, with a total integrated charge of 25 pC for the intermediate transient and 170 pC for the saturating transient.
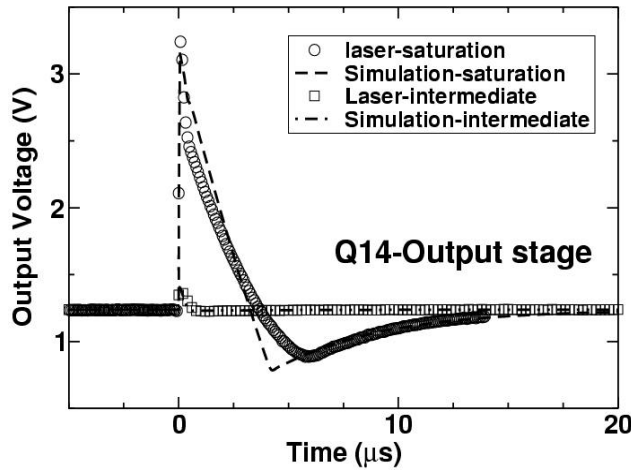


Fig. 7(c) Output voltage transients for a laser strike to transistor Q14 in the output stage of the LM124. The laser was simulated by a current source applied at the Collector-Base junction, with a total integrated charge of 3 pC for the intermediate transient and 45 pC for the saturating transient.

## IV.  ION MICROBEAM VS. SIMULATION

With the satisfactory SET laser calibration and the refinements performed on transistor model junction capacitances, the issue of the sensitivity of the circuit to actual heavy ions can be addressed. Previous work has shown that even though laser testing is a very powerful tool for SET analysis, it generates charge tracks that are not identical to those produced by heavy ion irradiation [16]. For example, issues such as laser penetration depth and the inability to reach devices and junctions screened by metal lines can impact direct reproduction of heavy ion effects. However, we will demonstrate that a judicious laser-based SET calibration of circuit electrical models (as outlined here) can achieve sensitivities identical to those resulting from heavy ion for a very comparable modeled collected charge.

The ion microbeam tests were performed at Sandia National Laboratories. The experimental setup consisted of a magnetically focussed ion beam, generated by a Tandem Van de Graaff particle accelerator. In our experiment, we used 40Mev Chlorine, having a surface LET of 18MeV/mg/cm$^2$ [7]. The resulting deposited charge in the silicon was estimated to be 1.2 pC. The circuit configuration used was similar to the laser beam experiments (Fig. 5).

To simulate the charge generated in the semiconductor by heavy ion strikes, we used current sources that we applied at the chosen junctions of targeted transistors. We should point out that it is vitally important that properly calibrated base, collector, and emitter spreading resistances be included in the transistor models and that the SET simulated current be induced across the device junction (not the device terminals) [8]. We found that, depending on the type of transistors, errors on the order of 10 to 35% in simulated critical charge were induced if this procedure was not followed. The following figures show a comparison between ion microbeam and simulation on several transistors of the circuit (Q3, Q5 and Q18). Results comparing ion microbeam with simulations are presented more exhaustively by R. Pease et al. [7].
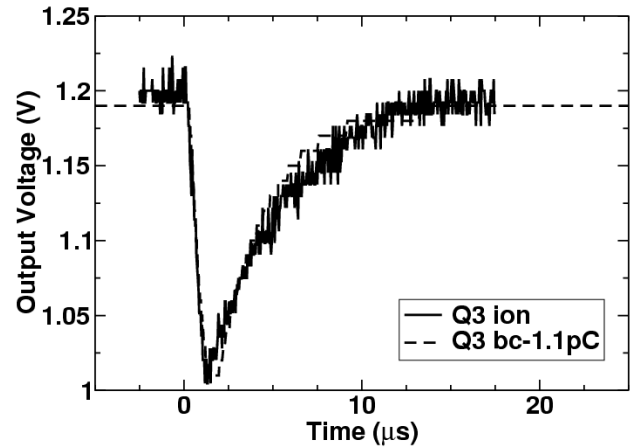


Fig. 8 (a) Comparison of SETs observed at the output of the LM124. The experimental curve "ion" was obtained by exposing transistor Q3 to the ion microbeam. The simulated curve indicates the junction and the charge that needs to be injected to match the experiment.

Fig. 8 (b) Comparison of SETs observed at the output of the LM124. The experimental curve "ion" was obtained by exposing transistor Q5 to the ion microbeam. The simulated curve indicates the junction and the charge that needs to be injected to match the experiment.
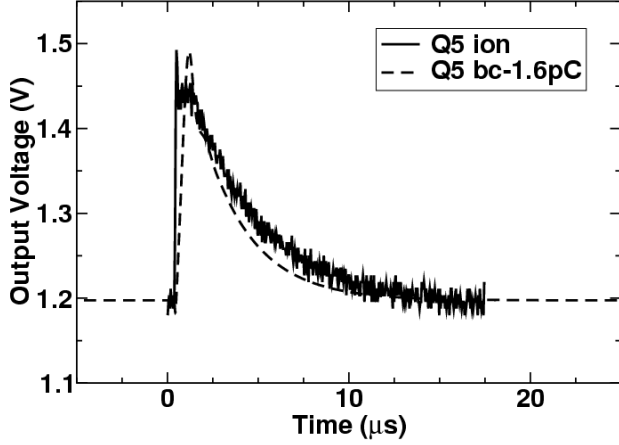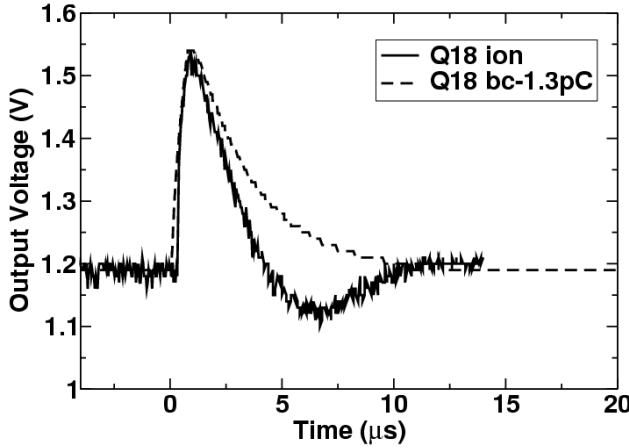


Fig. 8 (c) Comparison of SETs observed at the output of the LM124. The experimental curve "ion" was obtained by exposing transistor Q18 to the ion microbeam. The simulated curve indicates the junction and the charge that needs to be injected to match the experiment.

Fig. 8 illustrates the excellent correlation in the simulated and experimental SET waveforms observed at the output of the LM124. Very good agreement in the required collected charge to produce those transients is also observed.

## V. VALIDATION OF THE LM124 MODEL

A last key validation is needed to confidently present the LM124 model as adequate for SET *prediction* in space environments: a comparison to broad-beam experiments. Being able to adequately model SETs with a collected charge comparable to that of the microbeam ion is very encouraging. However, the microbeam is limited in the amount of charge it can deposit: it is restricted to low energy ions (maximum of 50MeV). So, broad beam testing is more suitable to reproduce a space environment.

Broad beam tests have been performed on the LM124 at Brookhaven National Laboratory in a circuit configuration different from that used in laser calibration. The circuit was a

non-inverting configuration with a closed loop gain of 2 as shown in Fig. 8. Using a different configuration than in the previous experiments allowed us to test the predictive abilities of the LM124, hence showing that the accuracy of the model is not dependant on the circuit configuration used during laser calibration (inverting with gain of 20). It is important that the accuracy of any model not be embedded in a specific test case; the model should be applicable in an unrestricted way. For simulation purposes, current sources were applied on each of the transistors junctions to reproduce the charge deposited by the ions. No additional fitting or calibration was performed on the laser-calibrated model of Section III.
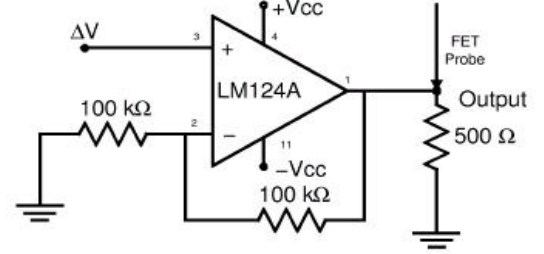


Fig. 9 LM124 non-inverting circuit configuration used in broad-beam tests.

Unlike laser beam irradiation and ion microbeam testing that target specific transistors and junctions, broadbeam experiment is characterized by the randomness of ion strike locations. Translating this experimental constraint to an equivalent computer-generated environment required an intensive computational effort. Since all the transistors of the circuit and their multiple junctions are possible targets, current sources modeling ion-induced transient currents were swept junction by junction across every transistor terminals where a charge collection process could occur: emitter-base junction, collector-base junction, emitter-collector shunt collector-substrate junction. We did not apply simultaneously multiple current sources to the circuit nodes to account for multiple ions strikes. Since the flux of particles during the broadbeam test was 110 particles/s (average of 1 hit every 9 milliseconds) and the duration of the SETs observed experimentally was over two order of magnitude faster, here is a very low probability of overlap between two consecutive pulses. The integrated charge of the current sources was swept from 0.1 pC to 10 pC and applied directly to the junction capacitance, to avoid once again the voltage drops across the spreading resistances at the terminals.

Fig. 10 and 11 show respectively broad beam results and simulations performed on the LM124 in the non-inverting configuration. In Fig.10, we plot the SET pulse amplitude as a function of the pulse width for transients generated by heavy ions under a range of irradiation conditions (see figure caption). This type of plot provides a convenient characterization of the SETs generated by a microcircuit following a heavy ion irradiation. In figure 11, we plot the same information for SETs produced by simulation for the junctions of the transistor-level circuit model. These figures

illustrate that the simulation results exhibit the same general characteristics as the experimental broadbeam data. They correlate to heavy ion data by presenting similar trends, output voltage swings and transients time-widths.
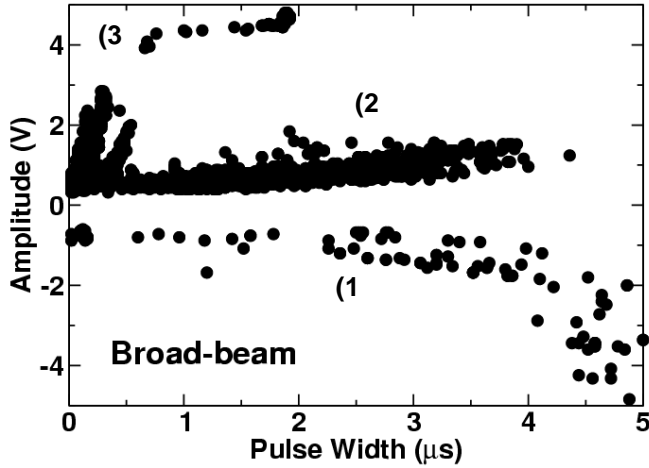


Fig. 10 Each point on the plots is representative of the amplitude vs. time-width at half maximum of amplitude (FWHM) of a SET observed at the output of the LM124 resulting from broad-beam experiments. The ions used during the experiment are 100MeV Br, 150 MeV Mg and 210 MeV Cl for angled strikes varying from $0^o$ to $60^o$. The corresponding LETs values of the ions used are 38.6, 6.25 and 11.5 MeV.$cm^2$/mg respectively.
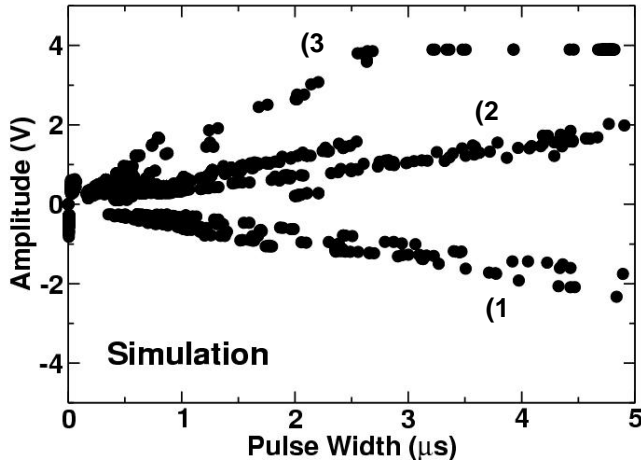


Fig. 11 Simulations results of laser-calibrated model plotting amplitude vs. time-width at half maximum of amplitude (FWHM) of observed output voltage transients. The integrated charge of the current sources used to produce the stimuli was varied from 0.1 to 10pC.

A further detailed analysis of the simulated results allows us to identify the circuit transistors that are responsible for the three distinct SET trends observed in the experimental data - 1) slowly increasing with negative amplitude, 2) slowly increasing with positive amplitude and 3) quickly increasing positive amplitude followed by a saturation effect. Since simulations allow a direct, unambiguous track of cause to effect, we were able to correlate the output pulses shown in Fig. 11 with the individual junctions causing the response. We have determined that type 1) SETs are mainly due to the transistors of the amplifier stage, while type 2) transients result from ion impacts on the input stage and, finally type 3) saturating transients are attributed to an extremely sensitive

part of the device located in the amplifier stage - which consists in a floating base NPN transistor used for temperature compensation, described in detail in [8]. Additional SETs labeled as glitches in the output voltage were also observed. Simulations determined that they were attributed to the output stage of the circuit.

This exercise demonstrates two of the most powerful utilities of models such as presented here. First, the ability to predict the response of a circuit to SETs in an application environment different from that in which the model was developed or calibrated. This is a key to model usefulness in time and cost savings. Second, the ability to interpret test data and discern cause to effect. The classification of the broadbeam trends shown in Fig. 10 to specific regions of the circuit would either be impossible, or at least very difficult and time consuming, without the insight provided by this detailed model and coupled simulations.

## VI. SUMMARY AND CONCLUSIONS

We have presented an engineering approach for the effective modeling of an analog operational amplifier circuit for ASET predictions. Following a path of careful circuit topology extraction from layout information and device model extraction from test devices, coupled with large signal, small signal, judicious laser-based SET calibration, and ion microbeam charge optimization, we developed a predictive SET model for the LM124 operational amplifier. Our efforts show that datasheet circuit schematics and basic datasheet parameters are NOT sufficient to predictively model SETs in analog components. However, our efforts show that SET circuit models can be developed using a combination of probing and characterization techniques. Our results also show that laser-based SET testing can be a crucial element of calibration in analog model development and test. Using these techniques, we developed a circuit model for the LM124 that is predictive for ASET in space conditions. Verification of the model with electrical, laser, microbeam and broadbeam test data validated the model fidelity.

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